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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>23 May 2008</u>.

2a)☐ This action is **FINAL**.                2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-55</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-55</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All  b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date <u>05/23/2008</u>.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____

5)☐ Notice of Informal Patent Application

6)☐ Other: _____

## DETAILED ACTION

This first non-final action is in response to the Request for Continued Examination filing of 05/23/2008. Claims 1-55 are pending and have been considered as follows.

### *Claim Objections*

1.      Claims 2 & 4 are objected to because of the following informalities:

-   Claim 2 line 9 recites the term "being" which should be omitted;

-   Claim 4 line 9 recites the term "being" which should be omitted;

Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

2.      35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1, 10, 21, & 38 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

-   Claim 1 recites "an electronic component" comprising what appears to be nothing more than computer software modules which is non-statutory subject matter, thereby invoking 35 U.S.C. 101;

- Claim 10 recites "an integrated circuit" comprising what appears to be nothing more than computer software modules which is non-statutory subject matter, thereby invoking 35 U.S.C. 101;

- Claim 21 recites "an integrated circuit" comprising what appears to be nothing more than computer software modules which is non-statutory subject matter, thereby invoking 35 U.S.C. 101;

- Claim 38 recites "an electronic device" comprising what appears to be nothing more than computer software modules which is non-statutory subject matter, thereby invoking 35 U.S.C. 101;

*Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works, and a compilation or mere arrangement of data.*
*Both types of "descriptive material" are nonstatutory when claimed as descriptive material per se, 33 F.3d at 1360, 31 USPQ2d at 1759. When functional descriptive material is recorded on some computer-readable medium, it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare In re Lowry, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994)(discussing patentable weight of data structure limitations in the context of a statutory claim to a data structure stored on a computer readable medium that increases computer efficiency) and >In re< Warmerdam, 33 F.3d *>1354,< 1360-61, 31 USPQ2d *>1754,< 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim) with Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory)*

### *Claim Rejections - 35 USC § 103*

3.     The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.     Claims 1 & 9 are rejected under 35 U.S.C. 102(b) as being unpatentable over <u>Tomasz et</u>

<u>al.</u> (US-6031878-A).

Claim 1:

<u>Tomasz et al.</u> disclose an electronic component comprising,

- "a tuning module of the direct sampling type that is able to receive satellite digital

  television analog signals composed of several channels" (i.e. "the tuner unit will have an

  input connector 56 for receiving the signal on cable 54, and an output connector 58 which

  may be used for coupling the received signal to a second set top box, if needed") [column

  3 lines 5-8];

- "several channel decoding digital modules connected at an output of the tuning module

  so as to deliver respectively simultaneously several streams of data packets

  corresponding to several different selected channels" (i.e. "The integrated circuit includes

  a variable gain amplifier 66, which amplifier will be more fully described in detail later

  herein, which provides a wide range of automatic gain control and high linearity to

  provide acceptably low cross-talk between channels in the output thereof. The output of

the amplifier 66 of course is a broadband output, containing in the preferred embodiment,

all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines

19-27];

but, they do not explicitly disclose,

- "an integrated circuit embodied on a single monolithic substrate," although Tomasz et al.

    do suggest integration of some elements, as recited below;

- "wherein analog and digital circuitry of both the tuning module and the several channel

    decoding modules are fabricated on that single monolithic substrate," although Tomasz et

    al. do suggest integration of some elements, as recited below;

however, Tomasz et al. do disclose,

- "the preferred embodiment by a single integrated circuit, so as to eliminate many

    components required or at least used in prior art systems to obtain and process the signal"

    [column 2 lines 59-62];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "an integrated circuit embodied on a single monolithic

substrate," in the invention as disclosed by Tomasz et al. since it would be reasonable to expect

that various separate components may be placed together for the purposes of integration.

Claim 9:

<u>Tomasz et al.</u> disclose an electronic component, as in Claim 1 above, further comprising,

-   "the electronic component comprises a satellite digital television signal receiver" (i.e.
    "The direct broadcast satellite signal received from the satellite dish is amplified and then
    downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite
    dish assembly, to a predetermined frequency band, typically in the L-band in the range
    950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

5.      Claims 2, 10, 11, 13-15, 20, 38, 48-50, & 55 are rejected under 35 U.S.C. 103(a) as being
unpatentable over <u>Tomasz et al.</u> (US-6031878-A) in view of <u>Robbins et al.</u> (US-6147713-A).

Claim 2:

<u>Tomasz et al.</u> disclose an electronic component, as in Claim 1 above, further comprising,

-   "the channels extend over a predetermined frequency span" (i.e. "all the channels in the
    950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];

-   "the analog signals convey digital information coded by digital modulation" (i.e.
    "Whether discrete filters or active filters are used, the output of the filters will be
    digitized by analog to digital converters 100 and then demodulated by the DSP for
    recovery of the digital data") [column 4 lines 58-61];

-   "the tuning module comprises: an analog stage receiving the said analog signals" (i.e.
    "the tuner unit will have an input connector 56 for receiving the signal on cable")
    [column 3 lines 5-6];

-    "the tuning module comprises: a multibit analog/digital conversion stage having a

     sampling frequency equal to at least twice the said frequency span" (i.e. "The level of the

     local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The

     signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as

     high as 20 dBm greater than the signal of interest. In order to avoid saturation of the

     amplifiers on the output of the mixers, feedback of the DC offset is provided from the

     amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset

     correction circuitry in general is well known, and need not be described in detail herein")

     [column 4 lines 43-52];

but, Tomasz et al. do not disclose,

-    "the tuning module comprises: several digital devices for transposing frequencies that are

     connected to the output of the analog conversion stage, each digital device being

     configured to separately deliver a sampled digital signal centered around the zero

     frequency and corresponding to a selected channel," although Robbins et al. do suggest

     utilizing a lowpass Nyquist filter and downconcerting, as recited below;

however, Robbins et al. do disclose,

-    "This signal is input both to a mixer and Nyquist filter block 72 and the carrier recovery

     block 74. In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered

     via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered

     carrier in mixer 82. The recovered carrier is first passed through a Nyquist delay 84

which compensates for the delay of the Nyquist filter 80. The Nyquist filter is a lowpass

filter that provides additional adjacent channel filtering as well as VSB double-single

sideband magnitude equalization" [column 7 lines 8-17];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the tuning module comprises: several digital devices for

transposing frequencies that are connected to the output of the analog conversion stage, each

digital device being configured to separately deliver a sampled digital signal centered around the

zero frequency and corresponding to a selected channel," in the invention as disclosed by

Tomasz et al. for the purposes of providing additional channel filtering.

Claim 10:

Tomasz et al. disclose an integrated circuit comprising,

- "a single monolithic substrate" (i.e. "the preferred embodiment by a single integrated

  circuit, so as to eliminate many components required or at least used in prior art systems

  to obtain and process the signal") [column 2 lines 59-62];

- "an input receiving an analog signal including a plurality of channels" (i.e. "the tuner unit

  will have an input connector 56 for receiving the signal on cable 54, and an output

  connector 58 which may be used for coupling the received signal to a second set top box,

  if needed") [column 3 lines 5-8];

- "a first channel decoding digital module connected to the first digital tuner that digitally

  decodes the first downconverted digital signal to output a stream of data packets for the

  selected first channel" (i.e. "The integrated circuit includes a variable gain amplifier 66,

  which amplifier will be more fully described in detail later herein, which provides a wide

range of automatic gain control and high linearity to provide acceptably low cross-talk between channels in the output thereof. The output of the amplifier 66 of course is a broadband output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27];

- "a second channel decoding digital module connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel" (i.e. "The integrated circuit includes a variable gain amplifier 66, which amplifier will be more fully described in detail later herein, which provides a wide range of automatic gain control and high linearity to provide acceptably low cross-talk between channels in the output thereof. The output of the amplifier 66 of course is a broadband output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27];

- "wherein circuitry of the converter, tuners and modules are fabricated on that single monolithic substrate" (i.e. "the preferred embodiment by a single integrated circuit, so as to eliminate many components required or at least used in prior art systems to obtain and process the signal") [column 2 lines 59-62];

but, Tomasz et al. do not disclose,

- "an analog-to-digital converter to convert the analog signal to a digital signal," although Robbins et al. do suggest a television converter utilizing lowpass Nyquist filter and downconversions, as recited below;

- "a first digital tuner that downconverts the digital signal to a first downconverted digital
  signal," although <u>Robbins et al.</u> do suggest a television converter and downconversions,
  as recited below;

- "information of a selected first channel in the downconverted digital signal is centered at
  around zero frequency," although <u>Robbins et al.</u> do suggest utilizing a lowpass Nyquist
  filter and downconversions, as recited below;

- "a second digital tuner that downconverts the digital signal to a second downconverted
  digital signal," although <u>Robbins et al.</u> do suggest utilizing a lowpass Nyquist filter and
  downconversions, as recited below;

- "information of a selected second channel in the downconverted digital signal is centered
  at around zero frequency," although <u>Robbins et al.</u> do suggest utilizing a lowpass Nyquist
  filter and downconversions, as recited below;

however, <u>Robbins et al.</u> do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The
  converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry
  24" [column 5 lines 1-3];

- "In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist
  filter 80 and then downconverted to baseband by mixing it with the recovered carrier in
  mixer 82" [column 7 lines 9-12];

- "The Nyquist filter is a lowpass filter that provides additional adjacent channel filtering
  as well as VSB double-single sideband magnitude equalization. For NTSC signals, the
  double sideband component is from 0-0.75 MHz and the single sideband component is
  from 0.75-4.2 MHz" [column 7 lines 14-19];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "an analog-to-digital converter to convert the analog signal to a

digital signal" and "a first digital tuner that downconverts the digital signal to a first

downconverted digital signal" and "information of a selected first channel in the downconverted

digital signal is centered at around zero frequency" and "a second digital tuner that downconverts

the digital signal to a second downconverted digital signal" and "information of a selected

second channel in the downconverted digital signal is centered at around zero frequency," in the

invention as disclosed by Tomasz et al. for the purposes of timing and data recovery and

providing additional adjacent channel filtering. In addition, it is understood that a plurality of

decoders and tuners may be present in the system to handle multiple simultaneous signals.

Claim 11:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, further

comprising,

- "the first and second digital tuners are each of a direct sampling type which performs
  frequency transposition and channel selection in a digital domain" (i.e. "the tuner unit
  will have an input connector 56 for receiving the signal on cable 54, and an output
  connector 58 which may be used for coupling the received signal to a second set top box,
  if needed") [column 3 lines 5-8].

Claim 13:

<u>Tomasz et al.</u> and <u>Robbins et al.</u> disclose an integrated circuit, as in Claim 10 above, further

comprising,

- "the analog signal conveys information for the plurality of channels by digital

    modulation" (i.e. "Whether discrete filters or active filters are used, the output of the

    filters will be digitized by analog to digital converters 100 and then demodulated by the

    DSP for recovery of the digital data") [column 4 lines 58-61].

Claim 14:

<u>Tomasz et al.</u> and <u>Robbins et al.</u> disclose an integrated circuit, as in Claim 10 above, further

comprising,

- "the channels of the analog signal extend over a frequency span" (i.e. "all the channels in

    the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];

    "the analog-to-digital converter oversamples the received analog signal at a sampling

    frequency at least twice the frequency span" (i.e. "The level of the local oscillator signal

    in the RF signal input to the mixers is approximately -50 dBm. The signal present may be

    as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm

    greater than the signal of interest. In order to avoid saturation of the amplifiers on the

    output of the mixers, feedback of the DC offset is provided from the amplifier chain to

    the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in

    general is well known, and need not be described in detail herein") [column 4 lines 43-

    52].

Claim 15:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 14 above, further

comprising,

- "the analog signal comprises a satellite digital television analog signal" (i.e. "The direct

   broadcast satellite signal received from the satellite dish is amplified and then

   downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite

   dish assembly, to a predetermined frequency band, typically in the L-band in the range

   950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 20:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, further

comprising,

- "the integrated circuit is a component within a satellite digital television signal receiver"

   (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and

   then downshifted within the Low Noise Block (LNB), a subsystem contained with the

   satellite dish assembly, to a predetermined frequency band, typically in the L-band in the

   range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 38:

Tomasz et al. disclose an electronic device comprising,

- "an integrated circuit embodied on a single monolithic substrate" (i.e. "the preferred

   embodiment by a single integrated circuit, so as to eliminate many components required

   or at least used in prior art systems to obtain and process the signal") [column 2 lines 59-

   62];

- "a multi-channel direct sampling type tuner that receives an analog signal composed of several channels and outputs first and second channel digital signals" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable 54, and an output connector 58 which may be used for coupling the received signal to a second set top box, if needed") [column 3 lines 5-8];

- "wherein circuitry of both the tuner and the first and second channel decoders are fabricated on that single monolithic substrate" (i.e. "the preferred embodiment by a single integrated circuit, so as to eliminate many components required or at least used in prior art systems to obtain and process the signal") [column 2 lines 59-62];

but, Tomasz et al. do not disclose,

- "a first channel decoder that receives the first channel digital signal and outputs a first channel stream of data packets," although Robbins et al. do suggest television conversion, as recited below;

- "a second channel decoder that receives the second channel digital signal and outputs a second channel stream of data packets," although Robbins et al. do suggest television conversion, as recited below;

however, Robbins et al. do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24" [column 5 lines 1-3];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "a first channel decoder that receives the first channel digital

signal and outputs a first channel stream of data packets" and "a second channel decoder that

receives the second channel digital signal and outputs a second channel stream of data packets,"

in the invention as disclosed by Tomasz et al. for the purposes of timing and data recovery.

Claim 48:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further

comprising,

- "the analog signal conveys information for the plurality of channels by digital

  modulation" (i.e. "Whether discrete filters or active filters are used, the output of the

  filters will be digitized by analog to digital converters 100 and then demodulated by the

  DSP for recovery of the digital data") [column 4 lines 58-61].

Claim 49:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further

comprising,

- "the channels of the analog signal extend over a frequency span" (i.e. "all the channels in

  the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];

- "the analog-to-digital converter oversamples the received analog signal at a sampling

  frequency at least twice the frequency span" (i.e. "The level of the local oscillator signal

  in the RF signal input to the mixers is approximately -50 dBm. The signal present may be

  as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm

  greater than the signal of interest. In order to avoid saturation of the amplifiers on the

output of the mixers, feedback of the DC offset is provided from the amplifier chain to

the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in

general is well known, and need not be described in detail herein") [column 4 lines 43-

52].

Claim 50:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 49 above, further

comprising,

- "the analog signal comprises a satellite digital television analog signal" (i.e. "The direct

broadcast satellite signal received from the satellite dish is amplified and then

downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite

dish assembly, to a predetermined frequency band, typically in the L-band in the range

950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 55:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further

comprising,

- "the integrated circuit is a component within a satellite digital television signal receiver"

(i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and

then downshifted within the Low Noise Block (LNB), a subsystem contained with the

satellite dish assembly, to a predetermined frequency band, typically in the L-band in the

range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

6.      Claims 7 & 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Tomasz et</u>

<u>al.</u> (US-6031878-A) in view of <u>Lieber et al.</u> (US-5220164-A).

Claim 7:

<u>Tomasz et al.</u> disclose an electronic component, as in Claim 1 above, but do not disclose,

-    "a grounding metal plate glued to a rear face of the single monolithic substrate by a

     conducting glue," although <u>Lieber et al.</u> do suggest utilizing "an opaque photocathode, a

     microchannel plate (MCP) electron multiplier, and a phosphor coated anode covered with

     a metalized layer", as recited below;

however, <u>Lieber et al.</u> do disclose,

-    "The single detection element includes an opaque photocathode, a microchannel plate

     (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer"

     [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "a grounding metal plate glued to a rear face of the single

monolithic substrate by a conducting glue," in the invention as disclosed by <u>Tomasz et al.</u> for the

purposes of providing both imaging and ranging functions.

Claim 8:

<u>Tomasz et al.</u> disclose an electronic component, as in Claim 1 above, but do not disclose,

-    "the substrate has a first type of conductivity," although <u>Lieber et al.</u> do suggest "MCP is

     grounded, with the anode being biased positively relative to the MCP, and the

     photocathode being biased negatively relative to the MCP", as recited below;

- "circuitry of the tuning module and several channel decoding digital modules performing a digital processing are disposed in a part of the substrate that is insulated from the remaining part of the substrate providing analog circuitry of the tuning module by a semiconducting barrier having a second type of conductivity different from the first type of conductivity," although Lieber et al. do suggest grounded MCP, as recited below;

- "the semiconducting barrier is biased by a bias voltage different from that used for the insulated part of the substrate," although Lieber et al. do suggest "the anode being biased positively relative to the MCP, and the photocathode being biased negatively relative to the MCP", as recited below;

however, Lieber et al. do disclose,

- "The detection of the prompt electrical current is made through a transformer that couples the anode to a power supply" [column 3 lines 41-43];

- "The power supply biases the anode relative to the MCP and photocathode such that the MCP is grounded, with the anode being biased positively relative to the MCP, and the photocathode being biased negatively relative to the MCP" [column 3 lines 44-48];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the substrate has a first type of conductivity" and "elements performing a digital processing are disposed in a part of the substrate that is insulated from the remaining part of the substrate by a semiconducting barrier having a second type of conductivity different from the first type of conductivity" and "the semiconducting barrier is biased by a bias voltage different from that used for the insulated part of the substrate," in the invention as

disclosed by <u>Tomasz et al.</u> for the purposes of allowing the prompt anode current to be detected

without having to ground the anode and the use of a non-grounded anode significantly simplifies

the power supply circuitry.

7.      Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Tomasz et al.</u> (US-

6031878-A) in view of <u>Hwang et al.</u> (US-4894657-A).

Claim 3:

<u>Tomasz et al.</u> disclose an electronic component, as in Claim 1 above, further comprising,

-   "the channels extend over a predetermined frequency span" (i.e. "all the channels in the

    950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];

-   "the analog signals convey digital information coded by digital modulation" (i.e.

    "Whether discrete filters or active filters are used, the output of the filters will be

    digitized by analog to digital converters 100 and then demodulated by the DSP for

    recovery of the digital data") [column 4 lines 58-61];

-   "each channel decoding digital module comprises: a digital decimator filter followed by

    an additional digital filter for eliminating information of adjacent channels" (i.e. "the

    output of the VCO is fed back, divided down by the ratio of the expected carrier

    frequency of the desired channel to the frequency of the crystal oscillator and then

    compared to the crystal oscillator frequency. The deviation in the external voltage

    controlled oscillator frequency is used to control the tank circuit to readjust the output

    frequency of the voltage controlled oscillator") [column 3 lines 38-44];

but they do not disclose,

-   "each channel decoding module comprises: a digital error correction stage for delivering

    a stream of data packets corresponding to the information conveyed by the channel being

    processed by the channel decoding module," although Hwang et al. do suggest

    calibration/digital correction, as recited below;

however, Hwang et al. do disclose,

-   "The calibrator is employed due to the need for calibration (or digital correction) arising

    out of the nonlinearity that may be present in pipelined A/D converters with greater than

    8- or 9-bit resolution" [column 3 lines 26-30];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "each channel decoding module comprises: a digital error

correction stage for delivering a stream of data packets corresponding to the information

conveyed by the channel being processed by the channel decoding module," in the invention as

disclosed by Tomasz et al. for the purposes of digital correction.

8.      Claims 4-6, 16-18, & 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further

view of Hwang et al.  (US-4894657-A).

Claim 4:

Tomasz et al. disclose an electronic component, as in Claim 1 above, further comprising,

-   "the channels extend over a predetermined frequency span" (i.e. "all the channels in the

    950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];

- "the analog signals convey digital information coded by digital modulation" (i.e. "Whether discrete filters or active filters are used, the output of the filters will be digitized by analog to digital converters 100 and then demodulated by the DSP for recovery of the digital data") [column 4 lines 58-61];

- "the tuning module comprises: an analog stage receiving the said analog signals" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable") [column 3 lines 5-6];

- "the tuning module comprises: a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the said frequency span" (i.e. "The level of the local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm greater than the signal of interest. In order to avoid saturation of the amplifiers on the output of the mixers, feedback of the DC offset is provided from the amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in general is well known, and need not be described in detail herein") [column 4 lines 43-52];

- "each channel decoding module comprises: a digital decimator filter followed by an additional digital filter for eliminating information of adjacent channels" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the

crystal oscillator frequency. The deviation in the external voltage controlled oscillator

frequency is used to control the tank circuit to readjust the output frequency of the

voltage controlled oscillator") [column 3 lines 38-44];

but, they do not disclose,

- "the tuning module comprises: several digital devices for transposing frequencies that are

    connected to the output of the analog conversion stage, each digital device being

    configured to separately deliver a sampled digital signal centered around the zero

    frequency and corresponding to a selected channel," although Robbins et al. do suggest

    utilizing a lowpass Nyquist filter and downconversions, as recited below;

- "each channel decoding module comprises: a digital error correction stage for delivering

    a stream of data packets corresponding to the information conveyed by the channel

    associated with the sampled digital signal processed by this channel decoding module,"

    although Hwang et al. do suggest calibration/digital correction, as recited below;

however, Robbins et al. do disclose,

- "This signal is input both to a mixer and Nyquist filter block 72 and the carrier recovery

    block 74. In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered

    via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered

    carrier in mixer 82. The recovered carrier is first passed through a Nyquist delay 84

    which compensates for the delay of the Nyquist filter 80. The Nyquist filter is a lowpass

    filter that provides additional adjacent channel filtering as well as VSB double-single

    sideband magnitude equalization" [column 7 lines 8-17]];

where as, Hwang et al. do disclose,

- "The calibrator is employed due to the need for calibration (or digital correction) arising
  out of the nonlinearity that may be present in pipelined A/D converters with greater than
  8- or 9-bit resolution" [column 3 lines 26-30];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the
applicant's invention to include, "the tuning module comprises: several digital devices for
transposing frequencies that are connected to the output of the analog conversion stage, each
digital device being configured to separately deliver a sampled digital signal centered around the
zero frequency and corresponding to a selected channel" and "each channel decoding module
comprises: a digital error correction stage for delivering a stream of data packets corresponding
to the information conveyed by the channel associated with the sampled digital signal processed
by this channel decoding module," in the invention as disclosed by Tomasz et al. for the
purposes of channel filtering and digital correction.

Claim 5:

Tomasz et al., Robbins et al., and Hwang et al. disclose an electronic component, as in Claim 4
above, but their combination do not disclose,

- "the resolution of the analog/digital conversion stage is greater than or equal to 6 bits,"
  although Hwang et al. do suggest converting as many as ten bits, as recited below;

however, Hwang et al. do disclose,

- "accurate resolution of the output code from flash A/D subconverter 10 is desired, D/A
  converter 16 may be of the capacitive type, which is capable of converting as many as ten
  bits without being unduly tolerance-dependent" [column 3 lines 9-10];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the resolution of the analog/digital conversion stage is greater

than or equal to 6 bits," in the invention as disclosed by Tomasz et al. and Robbins et al. for the

purposes of achieving accurate resolution of the output and without being tolerance dependent.

Claim 6:

Tomasz et al., Robbins et al., and Hwang et al. disclose an electronic component, as in Claim 4

above, but their combination do not disclose,

- "the decimator filter is a low-pass filter whose cutoff frequency is of the order of twice

  the frequency half-width of a channel," although Robbins et al. do suggest a lowpass

  Nyquist filter, as recited below;

- "the cutoff frequency of the additional digital filter is of the order of the frequency half-

  width of a channel," although Robbins et al. do suggest a cutoff frequency that is roughly

  half the width of the channel, as recited below;

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass

  filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz,

  passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40

  dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the decimator filter is a low-pass filter whose cutoff frequency

is of the order of twice the frequency half-width of a channel" and "the cutoff frequency of the

additional digital filter is of the order of the frequency half-width of a channel," in the invention

as disclosed by <u>Tomasz et al.</u> and <u>Hwang et al.</u> for the purposes of providing additional adjacent

channel filtering as well as VSB double-single sideband magnitude equalization.

Claim 16:

<u>Tomasz et al.</u> and <u>Robbins et al.</u> disclose an integrated circuit, as in Claim 10 above, further

comprising,

- "a decimator filter that filters the downconverted digital signal to output digital signals
  relating to the selected channel and adjacent channel information" (i.e. "the output of the
  VCO is fed back, divided down by the ratio of the expected carrier frequency of the
  desired channel to the frequency of the crystal oscillator and then compared to the crystal
  oscillator frequency. The deviation in the external voltage controlled oscillator frequency
  is used to control the tank circuit to readjust the output frequency of the voltage
  controlled oscillator") [column 3 lines 38-44];

- "a digital filter that filters out the adjacent channel information" (i.e. "the output of the
  VCO is fed back, divided down by the ratio of the expected carrier frequency of the
  desired channel to the frequency of the crystal oscillator and then compared to the crystal
  oscillator frequency. The deviation in the external voltage controlled oscillator frequency
  is used to control the tank circuit to readjust the output frequency of the voltage
  controlled oscillator") [column 3 lines 38-44].

but they do not disclose,

-    "an error correction stage to produce the data packets from the selected channel

     information," although Hwang et al. do suggest calibration/digital correction, as recited

     below;

however, Hwang et al. do disclose,

-    "The calibrator is employed due to the need for calibration (or digital correction) arising

     out of the nonlinearity that may be present in pipelined A/D converters with greater than

     8- or 9-bit resolution" [column 3 lines 26-30];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "an error correction stage to produce the data packets from the

selected channel information," in the invention as disclosed by Tomasz et al. and Robbins et al.

for the purposes of digital correction.

Claim 17:

Tomasz et al., Robbins et al., and Hwang et al. disclose an integrated circuit, as in Claim 16

above, but their combination do not disclose,

-    "the decimator filter is a low pass filter having a cut-off frequency approximately equal to

     twice a frequency half width of a channel," although Robbins et al. do suggest a lowpass

     Nyquist filter, as recited below;

however, <u>Robbins et al.</u> do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass
  filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz,
  passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40
  dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the decimator filter is a low pass filter having a cut-off

frequency approximately equal to twice a frequency half width of a channel," in the invention as

disclosed by <u>Tomasz et al.</u> and <u>Hwang et al.</u> for the purposes of implementing a Nyquist filter as

a finite impulse response (FIR) lowpass filter.

Claim 18:

<u>Tomasz et al.</u>, <u>Robbins et al.</u>, and <u>Hwang et al.</u> disclose an integrated circuit, as in Claim 17

above, but their combination do not disclose,

- "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the
  frequency half width of the channel," although <u>Robbins et al.</u> do disclose a lowpass
  Nyquist filter having a cut-off frequency that is roughly half the width of the channel, as
  recited below;

however, <u>Robbins et al.</u> do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass
  filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz,
  passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40
  dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the digital filter is a Nyquist filter having a cut-off frequency

approximately equal to the frequency half width of the channel," in the invention as disclosed by

Tomasz et al. and Hwang et al. for the purposes of implementing a Nyquist filter as a finite

impulse response (FIR) lowpass filter.

Claim 51:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further

comprising,

- "a decimator filter that filters the downconverted digital signal to output digital signals
  relating to the selected channel and adjacent channel information" (i.e. "the output of the
  VCO is fed back, divided down by the ratio of the expected carrier frequency of the
  desired channel to the frequency of the crystal oscillator and then compared to the crystal
  oscillator frequency. The deviation in the external voltage controlled oscillator frequency
  is used to control the tank circuit to readjust the output frequency of the voltage
  controlled oscillator") [column 3 lines 38-44];

- "a digital filter that filters out the adjacent channel information" (i.e. "the output of the
  VCO is fed back, divided down by the ratio of the expected carrier frequency of the
  desired channel to the frequency of the crystal oscillator and then compared to the crystal
  oscillator frequency. The deviation in the external voltage controlled oscillator frequency
  is used to control the tank circuit to readjust the output frequency of the voltage
  controlled oscillator") [column 3 lines 38-44];

but their combination do not disclose,

- "an error correction stage to produce the data packets from the selected channel
   information," although <u>Hwang et al.</u> do suggest accurate resolution output, as recited
   below;

however, <u>Hwang et al.</u> do disclose,

- "accurate resolution of the output code from flash A/D subconverter 10 is desired, D/A
   converter 16 may be of the capacitive type, which is capable of converting as many as ten
   bits without being unduly tolerance-dependent" [column 3 lines 9-10];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "an error correction stage to produce the data packets from the

selected channel information," in the invention as disclosed by <u>Tomasz et al.</u> and <u>Robbins et al.</u>

for the purposes of converting as many as ten bits without being unduly tolerance-dependent.

Claim 52:

<u>Tomasz et al., Robbins et al.,</u> and <u>Hwang et al.</u> disclose an electronic device, as in Claim 51

above, but their combination do not disclose,

- "the decimator filter is a low pass filter having a cut-off frequency approximately equal to
   twice a frequency half width of a channel," although <u>Robbins et al.</u> do disclose a lowpass
   Nyquist filter having a cut-off frequency that is roughly half the width of the channel, as
   recited below;

however, <u>Robbins et al.</u> do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass

  filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz,

  passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40

  dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the decimator filter is a low pass filter having a cut-off

frequency approximately equal to twice a frequency half width of a channel," in the invention as

disclosed by <u>Tomasz et al.</u>, <u>Robbins et al.</u>, and <u>Hwang et al.</u> for the purposes of implementing a

Nyquist filter as a finite impulse response (FIR) lowpass filter.

Claim 53:

<u>Tomasz et al.</u>, <u>Robbins et al.</u>, and <u>Hwang et al.</u> disclose an electronic device, as in Claim 52

above, but their combination do not disclose,

- "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the

  frequency half width of the channel," although <u>Robbins et al.</u> do disclose a lowpass

  Nyquist filter having a cut-off frequency that is roughly half the width of the channel, as

  recited below;

however, <u>Robbins et al.</u> do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass

  filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz,

  passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40

  dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the digital filter is a Nyquist filter having a cut-off frequency

approximately equal to the frequency half width of the channel," in the invention as disclosed by

Tomasz et al., Robbins et al., and Hwang et al. for the purposes of implementing a Nyquist filter

as a finite impulse response (FIR) lowpass filter.

9.      Claims 21-28, 30-32, 37, 39, & 40-46 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and

in further view of Young (EP-0481543-A1).

Claim 21:

Tomasz et al. disclose an integrated circuit comprising,

- "a single monolithic substrate" (i.e. "the preferred embodiment by a single integrated

    circuit, so as to eliminate many components required or at least used in prior art systems

    to obtain and process the signal") [column 2 lines 59-62];

- "an input receiving an analog signal including a plurality of channels" (i.e. "the tuner unit

    will have an input connector 56 for receiving the signal on cable 54, and an output

    connector 58 which may be used for coupling the received signal to a second set top box,

    if needed") [column 3 lines 5-8];

- "a first channel decoding digital module connected to the first digital tuner that decodes

    the first downconverted digital signal to output a stream of data packets for the selected

    first channel" (i.e. "The integrated circuit includes a variable gain amplifier 66, which

    amplifier will be more fully described in detail later herein, which provides a wide range

    of automatic gain control and high linearity to provide acceptably low cross-talk between

channels in the output thereof. The output of the amplifier 66 of course is a broadband

output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150

MHz DBS signal bandwidth") [column 3 lines 19-27];

-   "a second channel decoding digital module connected to the second digital tuner that

    decodes the second downconverted digital signal to output a stream of data packets for

    the selected second channel" (i.e. "The integrated circuit includes a variable gain

    amplifier 66, which amplifier will be more fully described in detail later herein, which

    provides a wide range of automatic gain control and high linearity to provide acceptably

    low cross-talk between channels in the output thereof. The output of the amplifier 66 of

    course is a broadband output, containing in the preferred embodiment, all the channels in

    the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27];

-   "wherein circuitry of the converters, tuners, modules and switching circuit are fabricated

    on that single monolithic substrate" (i.e. "the preferred embodiment by a single integrated

    circuit, so as to eliminate many components required or at least used in prior art systems

    to obtain and process the signal") [column 2 lines 59-62];

but they do not disclose,

-   "a first analog-to-digital converter to convert the analog signal to a first digital signal,"

    although Robbins et al. do suggest television conversion, as recited below;

-   "a second analog-to-digital converter to convert the analog signal to a second digital

    signal," although Robbins et al. do suggest television conversion, as recited below;

-   "a first digital tuner that downconverts a received digital signal to a first downconverted

    digital signal," although Robbins et al. do suggest downconversions, as recited below;

- "information of a selected first channel in the downconverted digital signal is centered at around zero frequency," although <u>Robbins et al.</u> do suggest downconversions, as recited below;

- "a second digital tuner that downconverts a received digital signal to a second downconverted digital signal," although <u>Robbins et al.</u> do suggest downconversions, as recited below;

- "information of a selected second channel in the downconverted digital signal is centered at around zero frequency," although <u>Robbins et al.</u> do suggest utilizing lowpass Nyquist filter and downconversion, as recited below;

- "a switching circuit that selectively couples the first and second digital signals output from the first and second converters to the first and second digital tuners," although <u>Young</u> does suggest switching, as recited below;

however, <u>Robbins et al.</u> do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24" [column 5 lines 1-3];

- "In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered carrier in mixer 82" [column 7 lines 9-12];

- "The Nyquist filter is a lowpass filter that provides additional adjacent channel filtering as well as VSB double-single sideband magnitude equalization. For NTSC signals, the double sideband component is from 0-0.75 MHz and the single sideband component is from 0.75-4.2 MHz" [column 7 lines 14-19];

where as, <u>Young</u> does disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a moving contact which can connect an output to either of the inputs. The three switches are ganged together so that their outputs are either all connected to their first respective inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a first analog-to-digital converter to convert the analog signal to a first digital signal" and "a second analog-to-digital converter to convert the analog signal to a second digital signal" and "a first digital tuner that downconverts a received digital signal to a first downconverted digital signal" and "information of a selected first channel in the downconverted digital signal is centered at around zero frequency" and "a second digital tuner that downconverts a received digital signal to a second downconverted digital signal" and "information of a selected second channel in the downconverted digital signal is centered at around zero frequency" and "a second channel decoding digital module connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel" and "a switching circuit that selectively couples the first and second digital signals output from the first and second converters to the first and second

digital tuners," in the invention as disclosed by <u>Tomasz et al.</u> for the purposes of having the

outputs either all connected to their first respective inputs or to their second respective inputs

simultaneously.

Claim 22:

<u>Tomasz et al., Robbins et al.,</u> and <u>Young</u> disclose an integrated circuit, as in Claim 21 above,

but their combination do not disclose,

- "the first analog-to-digital converter is associated with analog signals in a first passband,"

    although <u>Robbins et al.</u> do suggest analog-to-digital television conversion, as recited

    below;

- "the second analog-to-digital converter is associated with analog signals in a second

    passband," although <u>Robbins et al.</u> do suggest analog-to-digital television conversion, as

    recited below;

however, <u>Robbins et al.</u> do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The

    converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry

    24. The video DSP demodulates and unscrambles video from an intermediate frequency

    (IF) carrier. The carrier can comprise, for example, a low IF frequency carrier such as a

    carrier centered at 9 MHz plus or minus 100 KHz. The video DSP consists of an analog-

    to-digital (A/D) converter 14, video demodulator 16, and a video descrambler 18"

    [column 5 lines 1-8];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the
applicant's invention to include, "the first analog-to-digital converter is associated with analog
signals in a first passband" and "the second analog-to-digital converter is associated with analog
signals in a second passband," in the invention as disclosed by Tomasz et al. and Young since it
is understood that there may be a plurality of analog to digital converters where each converter
would correspond with its own input.

Claims 23-27:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 22 above, but
their combination do not disclose,

-   "if the first and second channels are located in the first passband, the switching circuit
    selectively couples the first and second digital tuners to the first analog-to-digital
    converter," although Young do suggest multiple input, contacts, and switch, switching, as
    recited below;

-   "if the first and second channels are located in the second passband, the switching circuit
    selectively couples the first and second digital tuners to the second analog-to-digital
    converter," although Young do suggest multiple input, contacts, and switch, switching, as
    recited below;

-   "if the first channel is located in the first passband and the second channel is located in
    the second passband, the switching circuit selectively couples the first digital tuner to the
    first analog-to-digital converter and the second digital tuner to the second analog-to-
    digital converter," although Young do suggest multiple input, contacts, and switch,
    switching, as recited below;

- "if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first digital tuner to the second analog-to-digital converter and the second digital tuner to the first analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and switch, switching, as recited below;

- "a first filter tuned to the first passband that outputs the analog signal to the first analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and switch, switching, as recited below;

- "a second filter tuned to the second passband that outputs the analog signal to the second analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and switch, switching, as recited below;

however, <u>Young</u> do disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a moving contact which can connect an output to either of the inputs. The three switches are ganged together so that their outputs are either all connected to their first respective inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second digital tuners to the first analog-to-digital converter," in the invention as disclosed by <u>Tomasz et al.</u> and <u>Robbins et al.</u> for the purposes of having their outputs either all connected to their first respective inputs or to their second respective inputs simultaneously.

Claim 28:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above,

further disclosing,

- "the first and second digital tuners are each of a direct sampling type which performs

  frequency transposition and channel selection in a digital domain" (i.e. "the tuner unit

  will have an input connector 56 for receiving the signal on cable 54, and an output

  connector 58 which may be used for coupling the received signal to a second set top box,

  if needed") [column 3 lines 5-8].

Claim 30:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above,

further disclosing,

- "the analog signal conveys information for the plurality of channels by digital

  modulation" (i.e. "Whether discrete filters or active filters are used, the output of the

  filters will be digitized by analog to digital converters 100 and then demodulated by the

  DSP for recovery of the digital data") [column 4 lines 58-61].

Claim 31:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above,

further disclosing,

- "the channels of the analog signal applied to each analog-to-digital converter extend over

  a given frequency span" (i.e. "all the channels in the 950 MHz to 2150 MHz DBS signal

  bandwidth") [column 3 lines 26-27];

- "each analog-to-digital converter oversamples the received analog signal at a sampling frequency at least twice the given frequency span" (i.e. "The level of the local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm greater than the signal of interest. In order to avoid saturation of the amplifiers on the output of the mixers, feedback of the DC offset is provided from the amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in general is well known, and need not be described in detail herein") [column 4 lines 43-52].

Claim 32:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 31 above, further disclosing,

- "the analog signal comprises a satellite digital television analog signal" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 37:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above,

further disclosing,

- "the integrated circuit is a component within a satellite digital television signal receiver"

    (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and

    then downshifted within the Low Noise Block (LNB), a subsystem contained with the

    satellite dish assembly, to a predetermined frequency band, typically in the L-band in the

    range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claims 39 & 40:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, Robbins et

al. further disclosing,

- "at least one analog-to-digital converter to convert the received analog signal to a digital

    signal" (i.e. "An overall block diagram of the television converter is illustrated in FIG. 1.

    The converter includes a video DSP 12, audio DSP 26, and timing and data recovery

    circuitry 24") [column 5 lines 1-3];

- "a first frequency transposition circuit that downconverts the digital signal to the first

    channel digital signal" (i.e. "In the mixer and Nyquist filter block 72, the video IF is first

    Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it

    with the recovered carrier in mixer 82") [column 7 lines 9-12];

- "a second frequency transposition circuit that downconverts the digital signal to the
  second channel digital signal" (i.e. "In the mixer and Nyquist filter block 72, the video IF
  is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by
  mixing it with the recovered carrier in mixer 82") [column 7 lines 9-12];

- "the multi-channel direct sampling type tuner comprises a first and second analog-to-
  digital converter that convert the received analog signal to a first and second digital
  signal" (i.e. "An overall block diagram of the television converter is illustrated in FIG. 1.
  The converter includes a video DSP 12, audio DSP 26, and timing and data recovery
  circuitry 24") [column 5 lines 1-3];

but their combination do not disclose,

- "the multi-channel direct sampling type tuner comprises a switching circuit that
  selectively couples the first and second digital signals to the first and second frequency
  transposition circuits," although Young does suggest switching, as recited below;

however, Young does disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a
  moving contact which can connect an output to either of the inputs. The three switches
  are ganged together so that their outputs are either all connected to their first respective
  inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the multi-channel direct sampling type tuner comprises a

switching circuit that selectively couples the first and second digital signals to the first and

second frequency transposition circuits," in the invention as disclosed by <u>Tomasz et al.</u> and

<u>Robbins et al.</u> for the purposes of having their outputs either all connected to their first respective

inputs or to their second respective inputs simultaneously.

Claim 41:

<u>Tomasz et al.</u>, <u>Robbins et al.</u>, and <u>Young</u> disclose an electronic device, as in Claim 40 above, but

their combination do not disclose,

- "the first analog-to-digital converter is associated with analog signals in a first passband,"

    although <u>Robbins et al.</u> do suggest analog-to-digital television conversion, as recited

    below;

- "the second analog-to-digital converter is associated with analog signals in a second

    passband," although <u>Robbins et al.</u> do suggest analog-to-digital television conversion, as

    recited below;

however, <u>Robbins et al.</u> do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The

    converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry

    24. The video DSP demodulates and unscrambles video from an intermediate frequency

    (IF) carrier. The carrier can comprise, for example, a low IF frequency carrier such as a

    carrier centered at 9 MHz plus or minus 100 KHz. The video DSP consists of an analog-

    to-digital (A/D) converter 14, video demodulator 16, and a video descrambler 18"

    [column 5 lines 1-8];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the first analog-to-digital converter is associated with analog

signals in a first passband" and "the second analog-to-digital converter is associated with analog

signals in a second passband," in the invention as disclosed by <u>Tomasz et al.</u>, <u>Robbins et al.</u>, and

<u>Young</u> for the purposes of timing and data recovery.

Claims 42-46:

<u>Tomasz et al.</u>, <u>Robbins et al.</u> and <u>Young</u> disclose an electronic device, as in Claim 41 above, but

their combination do not disclose,

- "if the first and second channels are located in the first passband, the switching circuit

  selectively couples the first and second frequency transposition circuits to the first

  analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and

  switch, switching, as recited below;

- "if the first and second channels are located in the second passband, the switching circuit

  selectively couples the first and second frequency transposition circuits to the second

  analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and

  switch, switching, as recited below;

- "if the first channel is located in the first passband and the second channel is located in

  the second passband, the switching circuit selectively couples the first frequency

  transposition circuit to the first analog-to-digital converter and the second frequency

  transposition circuit to the second analog-to-digital converter," although <u>Young</u> do

  suggest multiple input, contacts, and switch, switching, as recited below;

- "if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first frequency transposition circuit to the second analog-to-digital converter and the second frequency transposition circuit to the first analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and switch, switching, as recited below;

- "a first filter tuned to the first passband that outputs the analog signal to the first analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and switch, switching, as recited below;

- "a second filter tuned to the second passband that outputs the analog signal to the second analog-to-digital converter," although <u>Young</u> do suggest multiple input, contacts, and switch, switching, as recited below;

however,  <u>Robbins et al.</u> do disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a moving contact which can connect an output to either of the inputs. The three switches are ganged together so that their outputs are either all connected to their first respective inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second frequency transposition circuits to the first analog-to-digital converter" and "if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second frequency transposition circuits to the second analog-to-digital converter" and "if the first channel is

located in the first passband and the second channel is located in the second passband, the

switching circuit selectively couples the first frequency transposition circuit to the first analog-

to-digital converter and the second frequency transposition circuit to the second analog-to-digital

converter" and "if the first channel is located in the second passband and the second channel is

located in the first passband, the switching circuit selectively couples the first frequency

transposition circuit to the second analog-to-digital converter and the second frequency

transposition circuit to the first analog-to-digital converter," in the invention as disclosed by

Tomasz et al., Robbins et al., and Young for the purposes of having their outputs either all

connected to their first respective inputs or to their second respective inputs simultaneously.

10.     Claims 12 & 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz

et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Dapper

et al. (US-6275990-B1).

Claim 12:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, but they do

not disclose,

- "the analog-to-digital converter oversamples the received analog signal," although

    Dapper et al. do suggest oversampling, as recited below;

however, Dapper et al. do disclose,

- "Sigma Delta converter 2840 achieves high resolution by oversampling the input signal at

    a frequency much above the Nyquist frequency" [column 94 lines 23-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the analog-to-digital converter oversamples the received

analog signal," in the invention as disclosed by <u>Tomasz et al.</u> and <u>Robbins et al.</u> for the purposes

of achieving high resolution.

Claim 47:

<u>Tomasz et al.</u> and <u>Robbins et al.</u> disclose an electronic device, as in Claim 38 above, but they do

not disclose,

- "the analog-to-digital converter oversamples the received analog signal," although

   <u>Dapper et al.</u> do suggest oversampling, as recited below;

however, <u>Dapper et al.</u> do disclose,

- "Sigma Delta converter 2840 achieves high resolution by oversampling the input signal at

   a frequency much above the Nyquist frequency" [column 94 lines 23-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the analog-to-digital converter oversamples the received

analog signal," in the invention as disclosed by <u>Tomasz et al.</u> and <u>Robbins et al.</u> for the purposes

of achieving high resolution.

11.     Claims 19 & 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Tomasz</u>

<u>et al.</u> (US-6031878-A) in view of <u>Robbins et al.</u> (US-6147713-A) and in further view of <u>Lieber et</u>

<u>al.</u> (US-5220164-A).

Claim 19:

<u>Tomasz et al.</u> and <u>Robbins et al.</u> disclose an integrated circuit, as in Claim 10 above, but they do

not disclose,

- "a metal plate attached to a rear surface of the single monolithic substrate," although
  Lieber et al. do suggest "an opaque photocathode, a microchannel plate (MCP) electron
  multiplier, and a phosphor coated anode covered with a metalized layer", as recited
  below;

however, Lieber et al. do disclose,

- "The single detection element includes an opaque photocathode, a microchannel plate
  (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer"
  [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the
applicant's invention to include, "a metal plate attached to a rear surface of the single monolithic
substrate," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of
allowing some of the electrons striking the anode to be detected as a prompt electrical current.

Claim 54:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, but they do
not disclose,

- "a metal plate attached to a rear surface of the single monolithic substrate," although
  Lieber et al. do suggest "an opaque photocathode, a microchannel plate (MCP) electron
  multiplier, and a phosphor coated anode covered with a metalized layer", as recited
  below;

however, Lieber et al. do disclose,

- "The single detection element includes an opaque photocathode, a microchannel plate

    (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer"

    [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "a metal plate attached to a rear surface of the single monolithic

substrate," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of

allowing some of the electrons striking the anode to be detected as a prompt electrical current.

12.     Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al.

(US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Young  (EP-

0481543-A1) and in further view of Dapper et al. (US-6275990-B1).

Claim 29:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, but

they do not disclose,

- "each analog-to-digital converter oversamples the received analog signal," although

    Dapper et al. do suggest oversampling, as recited below;

however, Dapper et al. do disclose,

- "Sigma Delta converter 2840 achieves high resolution by oversampling the input signal at

    a frequency much above the Nyquist frequency" [column 94 lines 23-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "each analog-to-digital converter oversamples the received

analog signal," in the invention as disclosed by <u>Tomasz et al.</u>, <u>Robbins et al.</u>, and <u>Young</u> for the

purposes of achieving high resolution.

13.     Claim 33-35 is rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Tomasz et al.</u>

(US-6031878-A) in view of <u>Robbins et al.</u> (US-6147713-A) and in further view of <u>Young</u> (EP-

0481543-A1) and in further view of <u>Hwang et al.</u> (US-4894657-A).

Claim 33:

<u>Tomasz et al.</u>, <u>Robbins et al.</u>, and <u>Young</u> disclose an integrated circuit, as in Claim 21 above,

further disclosing,

-     "a decimator filter that filters the downconverted digital signal to output digital signals

      relating to the selected channel and adjacent channel information" (i.e. "the output of the

      VCO is fed back, divided down by the ratio of the expected carrier frequency of the

      desired channel to the frequency of the crystal oscillator and then compared to the crystal

      oscillator frequency. The deviation in the external voltage controlled oscillator frequency

      is used to control the tank circuit to readjust the output frequency of the voltage

      controlled oscillator") [column 3 lines 38-44];

-     "a digital filter that filters out the adjacent channel information" (i.e. "the output of the

      VCO is fed back, divided down by the ratio of the expected carrier frequency of the

      desired channel to the frequency of the crystal oscillator and then compared to the crystal

oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

but they do not disclose,

- "an error correction stage to produce the data packets from the selected channel information," although Hwang et al. do suggest "accurate resolution" output, as recited below;

however, Hwang et al. do disclose,

- "accurate resolution of the output code from flash A/D subconverter 10 is desired, D/A converter 16 may be of the capacitive type, which is capable of converting as many as ten bits without being unduly tolerance-dependent" [column 3 lines 9-10];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "an error correction stage to produce the data packets from the selected channel information," in the invention as disclosed by Tomasz et al., Robbins et al., and Young for the purposes of converting as many as ten bits without being unduly tolerance-dependent.

Claim 34:

Tomasz et al., Robbins et al., Young, and Hwang et al. disclose an integrated circuit, as in Claim

33 above, but their combination do not disclose,

- "the decimator filter is a low pass filter having a cut-off frequency approximately equal to

  twice a frequency half width of a channel," although Robbins et al. do suggest lowpass

  Nyquist filter with a cut-off frequency roughly half the width of a channel, as recited

  below;

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass

  filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz,

  passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40

  dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the decimator filter is a low pass filter having a cut-off

frequency approximately equal to twice a frequency half width of a channel," in the invention as

disclosed by Tomasz et al., Young, and Hwang et al. for the purposes of implementing a Nyquist

filter as a finite impulse response (FIR) lowpass filter.

Claim 35:

Tomasz et al., Robbins et al., Young, and Hwang et al. disclose an integrated circuit, as in Claim

34 above, but their combination do not disclose,

- "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the

    frequency half width of the channel," although Robbins et al. do suggest lowpass Nyquist

    filter with a cut-off frequency roughly half the width of a channel, as recited below;

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass

    filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz,

    passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40

    dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the digital filter is a Nyquist filter having a cut-off frequency

approximately equal to the frequency half width of the channel," in the invention as disclosed by

Tomasz et al., Young, and Hwang et al. for the purposes of implementing a Nyquist filter as a

finite impulse response (FIR) lowpass filter.

14.     Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al.

(US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Young  (EP-

0481543-A1) and in further view of Lieber et al. (US-5220164-A).

Claim 36:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, but

they do not disclose,

- "a metal plate attached to a rear surface of the single monolithic substrate," <u>Lieber et al.</u>

   do suggest "an opaque photocathode, a microchannel plate (MCP) electron multiplier,

   and a phosphor coated anode covered with a metalized layer", as recited below;

however, <u>Lieber et al.</u> do disclose,

- "The single detection element includes an opaque photocathode, a microchannel plate

   (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer"

   [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "a metal plate attached to a rear surface of the single monolithic

substrate," in the invention as disclosed by <u>Tomasz et al.</u>, <u>Robbins et al.</u>, and <u>Young</u> for the

purposes of allowing some of the electrons striking the anode to be detected as a prompt

electrical current.


### *Response to Arguments*

15.     Applicant's arguments filed 05/23/2008 have been fully considered but they are not

persuasive.

- The applicant's remark with respect to "<u>Tomasz</u> only disclosing analog downconversion

   and tuning functionality" has been carefully considered but is non-persuasive;

   o   The examiner notes that there is enough suggestion provided by the prior art of

       record <u>Tomasz</u> either independently or in combination that it would be reasonable

       to have either analog or digital tuning/conversions/modulation/etc;

- The applicant's remark regarding independent Claims 1, 10, 21, & 38 and their

  dependents stating that the prior art of record individually or in any combination do not

  disclose all of the integrated circuit limitations as part of the same single monolithic

  substrate, has been carefully considered but is non-persuasive;

  o The examiner notes that it is obvious as to whether the individual modules/circuit

    components reside as integrated together or as separate parts.

    *In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) (A claim to a
    fluid transporting vehicle was rejected as obvious over a prior art reference which
    differed from the prior art in claiming a brake drum integral with a clamping means,
    whereas the brake disc and clamp of the prior art comprise several parts rigidly secured
    together as a single unit. The court affirmed the rejection holding, among other reasons,
    "that the use of a one piece construction instead of the structure disclosed in [the prior
    art] would be merely a matter of obvious engineering choice.")*

- The applicant's remark with respect to the switches of <u>Young</u> not material to the claimed

  invention has been carefully considered but is non-persuasive;

  o The examiner's intended purpose/logic to the usage of <u>Young</u> was to show that

    switches, regardless what they may be used for, still perform same/similar

    functions (i.e. switching thereby connecting one part with another);

### *Conclusion*

16.    Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2100 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

OAL
07/23/2008

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